
EXHIBIT 2

Trials@uspto.gov
571-272-7822

Paper 13
Entered: June 22, 2022

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

STMICROELECTRONICS, INC.,
Petitioner,

v.

THE TRUSTEES OF PURDUE UNIVERSITY,
Patent Owner.

IPR2022-00252
Patent 7,498,633 B2

Before GRACE KARAFFA OBERMANN, JO-ANNE M. KOKOSKI,
and JEFFREY W. ABRAHAM, *Administrative Patent Judges*.

OBERMANN, *Administrative Patent Judge*.

DECISION
Denying Institution of *Inter Partes* Review
35 U.S.C. § 314

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I. INTRODUCTION

Petitioner¹ filed a Petition (Paper 2, “Pet.”) for institution of an *inter partes* review of claims 9–11 of U.S. Patent No. 7,498,633 B2 (Ex. 1001, “the ’633 patent”). Patent Owner² filed a Preliminary Response. Paper 8 (“Prelim. Resp.”). The parties identify two district court actions as related matters: *The Trustees of Purdue University v. STMicroelectronics N.V., et al.*, No. 6:21-CV-00727 (W.D. Tex.) and *The Trustees of Purdue University v. Wolfspeed, Inc.*, No. 1:21-CV-840 (M.D.N.C.). Pet. 1–2; Paper 4, 1.

II. BACKGROUND

A. The ’633 Patent (Ex. 1001)

The ’633 patent relates to a double-implanted metal-oxide semiconductor field effect transistor (“DIMOSFET”) having a substrate, drift layer, first source region, first source electrode, plurality of first base contact regions, second source region, second source electrode, plurality of second base contact regions, and junction field-effect transistor (“JFET”) region. Ex. 1001, 9:41–10:8.

According to the ’633 patent, “[o]ne design consideration in the fabrication of” metal-oxide semiconductor field effect transistors (“MOSFETs”) “is the blocking voltage of the semiconductor device.” *Id.* at 1:18–21. The blocking voltage is “the drain-to-source voltage of the” MOSFET “at which avalanche breakdown occurs and/or the strength of the

¹ The Petition identifies STMicroelectronics, Inc., STMicroelectronics N.V., and STMicroelectronics International N.V. as real parties-in-interest for Petitioner. Pet. 1.

² Patent Owner’s Mandatory Notice identifies The Trustees of Purdue University as the sole real party-in-interest for Patent Owner. Paper 4, 1.

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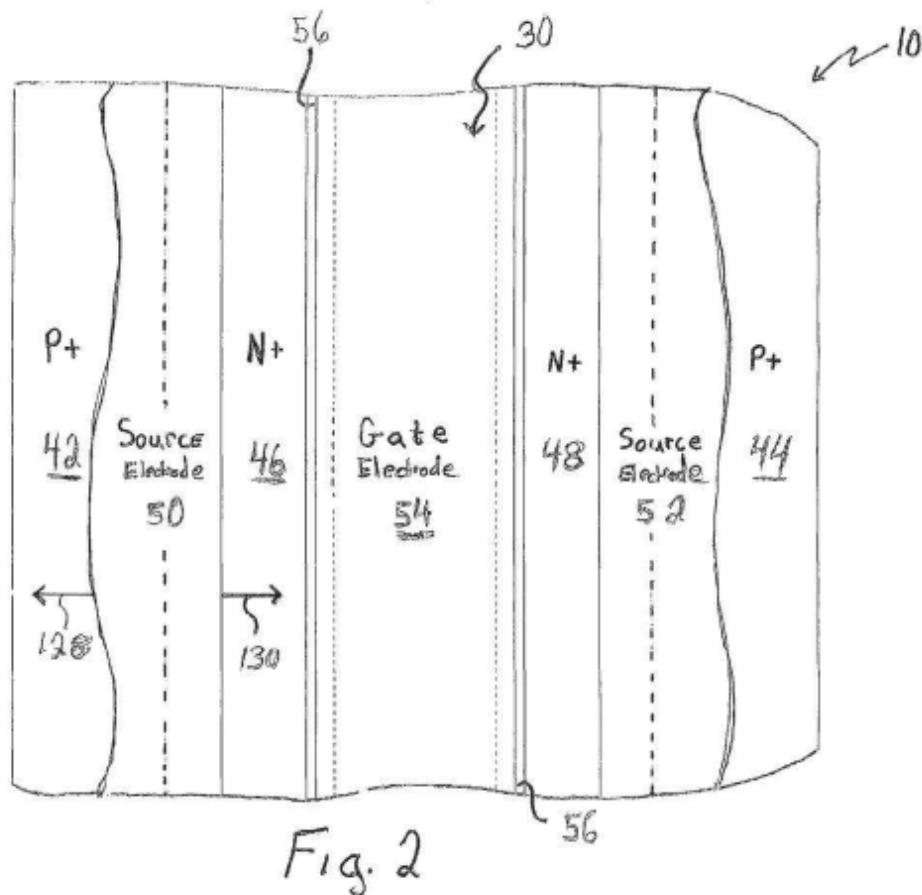
magnetic field of the gate oxide at which the gate oxide fails.” *Id.* at 1:21–25. For high-voltage power applications, a high blocking voltage generally is desirable. *Id.* at 1:25–27.

Another design consideration is “the specific on-resistance of the semiconductor device,” that is, “the product of the resistance of the device between the source and drain when the device is in an on-state and the area of the device.” *Id.* at 1:27–31. As the specific on-resistance decreases, efficiency of the semiconductor device may improve. *Id.* at 1:31–33. Typically, however, fabrication techniques that reduce the specific on-resistance of a high-voltage power MOSFET may also reduce the blocking voltage of the device. *Id.* at 1:33–36.

The DIMOSFET of the claimed invention includes a “first source electrode formed over the first source region, the first source electrode defining a longitudinal axis” and “a plurality of first base contact regions defined in the first source region, each of the plurality of first base contact regions being spaced apart from each other in a direction parallel to the longitudinal axis defined by the first source electrode.” *Id.* at 9:47–53 (claim 9). Similarly, the DIMOSFET includes a second source electrode formed over the first source region and a plurality of second base contact regions spaced apart from each other in a direction parallel to the longitudinal axis defined by the second source electrode. *Id.* at 9:55–10:5. The specified semiconductor device also includes a JFET region located between the first source region and the second source region and, in some embodiments, the JFET region has “a width less than about three micrometers.” *Id.* at 10:6–8 (claim 9). We next address advantages attributed to the claimed invention as described and illustrated in the ’633 patent.

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The '633 patent indicates that, at some point during the design process, “the specific on-resistance contribution JFET region of a MOSFET device is reduced to a point” where “the source resistance . . . becomes one of the dominating contributions to the specific on-resistance of the device.” *Id.* at 7:22–26. Manufacturing process variations, such as the topological configuration of Figure 2, reproduced below, may result in “an undesirable source resistance” if source regions 46 and 48 are misaligned with respect to base contact regions 42 and 44, or source regions 46 and 48 are misaligned with respect to source electrodes 50 and 52. *Id.* at 7:39–44.³



³ This disclosure misidentifies source region 52 as element 42. Compare Ex. 1001, 7:35–36 (correct numeric identifications), with *id.* at 7:44.

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Ex. 1001, Fig. 2. Figure 2 is a plan view of a portion of a semiconductor device of the claimed invention. *Id.* at 3:50–53. Figure 2 illustrates semiconductor device 10, including the locations of JFET region 30, gate electrode 54, source regions 46 and 48, which are doped with N-type (“N⁺”) impurities, base electrode regions 42 and 44, which are doped with P-type (“P⁺”) impurities, and source electrodes 50 and 52, which, respectively, are formed over source regions 46 and 48. *Id.* at 6:63–7:6.

“The source regions 46, 48 and base contact regions 42, 44 extend longitudinally with and substantially parallel to the source electrodes 50, 52 and the JFET region 30.” *Id.* at 7:35–38. The ’633 patent explains,

Because of semiconductor manufacturing process variations, such a topological configuration as illustrated in FIG. 2 can result in an undesirable source resistance if the source regions 46, 48 are misaligned with respect to the base contact regions 42, 44 and/or the source regions 46, 48 are misaligned with respect to the source electrodes 50, [5]2. For example, with respect to the source region 46, if the source electrode 50 is inadvertently formed more toward the direction of arrow 128 and/or the source region 46 is inadvertently formed more toward the direction of arrow 130, the source electrode 50 may not adequately cover the source region 46 and thereby cause the source resistance of the semiconductor device 10 to be increased due to the misalignment.

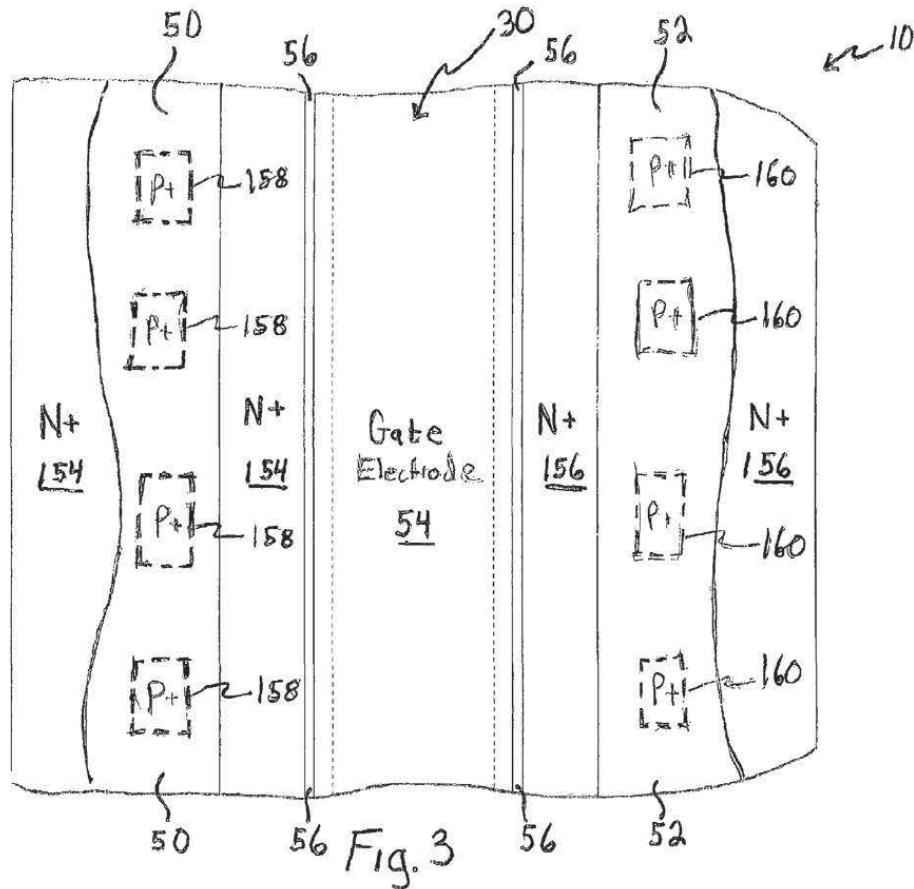
Id. at 7:39–51.

“[T]o reduce the likelihood of misalignment between the source electrodes and the source regions, the semiconductor device” of the claimed invention “is fabricated to have source regions” that each include a plurality of base contact regions, formed in the base source regions, respectively. *Id.* at 7:52–57. For example, the base contact regions may be “embodied as

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small ‘islands’ or regions within the larger source regions.” *Id.* at 7:57–59. Such a configuration is illustrated in Figure 3, which we reproduce below.



Ex. 1001, Fig. 3. Figure 3 is a plan view of an embodiment of the invention of the ’633 patent. *Id.* 3:54–54. Figure 3 illustrates semiconductor device 10, which includes base contact regions 158 and 160 that are “embodied as small ‘islands’ or regions within the larger source regions” denoted as elements 154 and 156. *Id.* at 7:57–59. “The base contact regions 158, 160 are formed to be located in a central location under the source metallic electrodes 50, 52 with areas of source regions 154, 156” that are “spaced between each base contact region.” *Id.* at 7:59–63. “Because the source regions 154, 156 form a greater portion of the area under the source electrodes 50, 52, the tolerance to manufacturing variability of the

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semiconductor device 10 may be increased.” *Id.* at 7:65–8:1. Thus, “even if the source electrodes 50, 52 are slightly misaligned with respect to the source regions 154, 156, the source resistance of the semiconductor device 10 is not substantially increased,” given that “a substantial portion of the source regions 154, 156 would remain aligned with the respective source electrode 50, 52.” *Id.* at 8:1–6.

The ’633 patent explains other advantages associated with the claimed invention by reference to Figure 1, which we reproduce below.

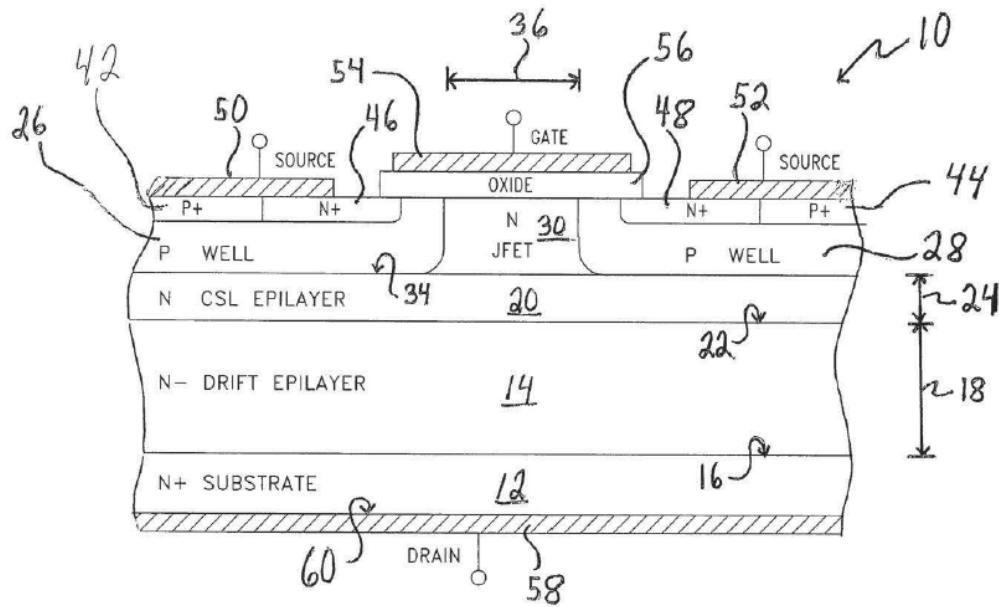


Fig. 1

Ex. 1001, Fig. 1. Figure 1 is a diagrammatic cross-sectional view of an embodiment of semiconductor device 10. According to the ’633 patent, JFET region 30 may be “fabricated to have a short width 36 relative to a typical DMOSFET device, which may reduce the specific on-resistance of the semiconductor device 10.” *Id.* at 6:21–24. For example, in some embodiments, “JFET region 30 has a width 36 that is about three micrometers or less.” *Id.* at 6:24–26 (referring to Figure 1).

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B. Challenged Claims

We reproduce below claim 9, which is the only independent claim challenged and illustrates the subject matter of the invention.

9. A double-implanted metal-oxide semiconductor field-effect transistor comprising:
 - a silicon-carbide substrate;
 - a drift semiconductor layer formed on a front side of the semiconductor substrate;
 - a first source region;
 - a first source electrode formed over the first source region, the first source electrode defining a longitudinal axis;
 - a plurality of first base contact regions defined in the first source region, each of the plurality of first base contact regions being spaced apart from each other in a direction parallel to the longitudinal axis defined by the first source electrode;
 - a second source region;
 - a second source electrode formed over the second source region, the second source electrode defining a longitudinal axis;
 - a plurality of second base contact regions defined in the second source region, each of the plurality of second base contact regions being spaced apart from each other in a direction parallel to the longitudinal axis defined by the second source electrode; and
 - a JFET region defined between the first source region and the second source region, the JFET region having a width less than about three micrometers.

Ex. 1001, 9:41–10:8.

Claims 10 and 11 depend from claim 9 and impose additional limitations on the JFET region. *Id.* at 10:9–18. Specifically, claim 10 specifies that “the JFET region has a width of about one micrometer.” *Id.* at 10:9–11. Claim 11, by contrast, imposes limitations pertaining to the relative concentrations of “first type impurities” included in the JFET region and drift semiconductor layer. *Id.* at 11:12–18.

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C. Single Ground of Unpatentability Asserted in the Petition

Petitioner advances a single ground of unpatentability based on information that the subject matter of claims 9–11 would have been obvious under 35 U.S.C. § 103(a)⁴ over the combined disclosures of Ryu⁵ (Ex. 1003) and Williams⁶ (Ex. 1004). Pet. 4. The challenge is supported by the Declaration of Dr. Vivek Subramanian (Ex. 1002).

III. ANALYSIS

We have authority to institute an *inter partes* review only where “there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a) (2018). The findings and conclusions set forth in this Decision are provided for the exclusive purpose of explaining our determination that Petitioner has not met that standard on this record.

A. Overview of the Prior Art

1. Ryu (Ex. 1003)

Ryu is titled “Vertical JFET Limited Silicon Carbide Power Metal-Oxide Semiconductor Field Effect Transistors and Methods of Fabricating Vertical JFET Limited Silicon Carbide Metal-Oxide Semiconductor Field Effect Transistors.” Ex. 1003, code (54). Ryu is concerned with

⁴ The Leahy-Smith America Invents Act (“AIA”), Pub. L. No. 112-29, 125 Stat. 284 (2011), revised 35 U.S.C. § 103 effective March 16, 2013. Because the ’633 patent has an effective filing date before March 16, 2013 (Ex. 1001, codes (22), (60), (65)), we refer to the pre-AIA version of Section 103.

⁵ U.S. Patent Publication No. 2004/0119076 A1, published June 24, 2004, filed October 30, 2003.

⁶ U.S. Patent 6,413,822 B2, issued July 2, 2002, filed April 22, 1999.

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“semiconductor devices” such as silicon carbide (SiC) MOSFETs. *Id.* ¶ 3.

Embodiments of SiC MOSFETs in Ryu “may reduce on-state resistance.”

Id. ¶ 39.

Ryu discloses an embodiment in which “a lightly doped n⁻ drift layer 12 of silicon carbide is on an optional n⁺ layer 10 of silicon carbide.”

Id. ¶ 40. We reproduce below Ryu’s Figure 2A.

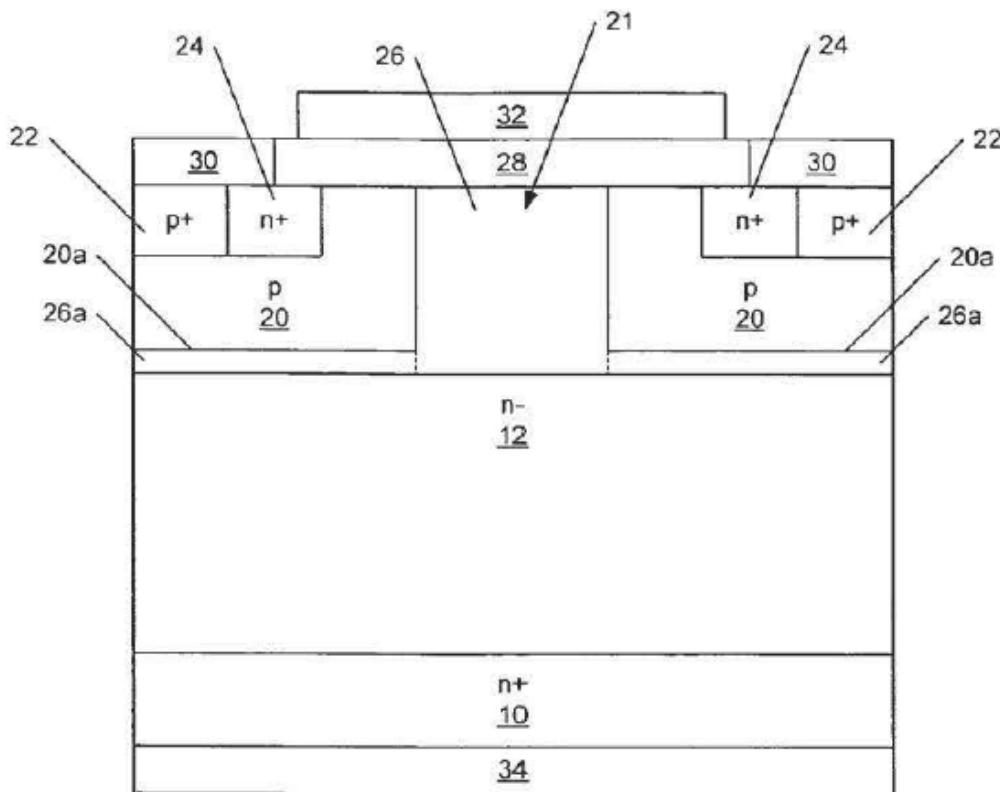


Figure 2A

Ex. 1003, Fig. 2A. Figure 2A of Ryu “is a cross-sectional view of a SiC MOSFET” and illustrates substrate layer 10 made of SiC and doped to an “n⁺” concentration. *Id.* ¶¶ 28, 40. Drift layer 12 on substrate layer 10 may be an epitaxial layer of SiC and doped to an “n⁻” concentration. *Id.* The gap between p-wells 20 “may be referred to as the JFET region 21.” *Id.* ¶ 44. Ryu discloses that “the gap 21 between the p-wells 20 has a higher carrier

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concentration than the drift layer 12.” *Id.* ¶ 42. Ryu explains, “If this gap is too high, the field in the gate oxide can become too high when the device is in the blocking state. However, if the gap is too narrow, the resistance of the JFET region 21 may become very high. Accordingly, gaps of from about 1 μm to about 10 μm are preferred.” *Id.* ¶ 44.

The MOSFET of Ryu includes n⁺ regions 24 and p⁺ regions 22 disposed within the p-wells 20. *Id.* ¶ 45. The n⁺ regions 24 are doped with n-type dopants to a “n⁺” concentration. *Id.* ¶¶ 6, 45. P⁺ regions 22 are adjacent to n⁺ regions 24 and formed by implanting p-type impurities to a “p⁺” concentration. *Id.* ¶ 55. Ryu discloses that source contacts 30 “provide an ohmic contact to both p⁺ regions 22 and n⁺ regions 24.” *Id.* ¶ 47.

2. Williams (Ex. 1004)

Williams is titled “Super-Self-Aligned Fabrication Process of Trench-Gate DMOS With Overlying Device Layer.” Ex. 1004, code (54). Williams discloses MOSFETs, noting that “the primary design goal for a power MOSFET used as a switch is to achieve the lowest on-resistance by simultaneously minimizing each of its resistive constituents.” *Id.* at 1:50–52. Williams further explains,

The channel resistance is minimized by maximizing the channel perimeter for a given area. The individual cells of the MOSFET may be constructed in any striped or polygonal shape. Ideally, the shape chosen should be one that can be repeated at a regular pitch so that more cells can be connected in parallel in a given area. By paralleling many cells and operating them in tandem an extremely low on-resistance can be achieved.

Id. at 2:1–8.

Figures 19A–19F of Williams disclose “plan views of various source-body designs.” *Id.* at 10:17–18. Williams explains that these figures show

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that “source and body contact construction can also be varied geometrically for the stripe design.” *Id.* at 16:28–30.

We reproduce below Williams’ Figure 19C.

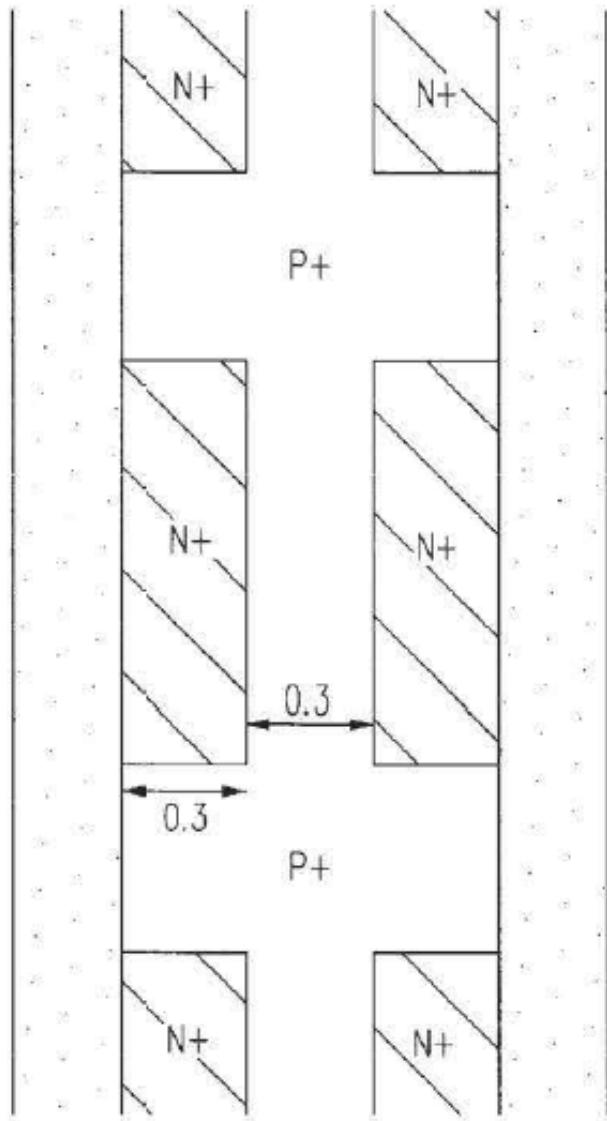


FIG. 19C

Ex. 1004, Fig. 19C. Figure 19C of Williams “shows continuous P⁺ body contact region with N⁺ source ‘islands.’” *Id.* at 10:21–22. Williams explains that “the segmented N⁺ source design of FIG. 19C reduces the N⁺ contact

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and the channel perimeter further, compromising on-resistance to achieve enhanced ruggedness.” *Id.* at 16:63–65.

We reproduce below Williams’ Figure 19E.

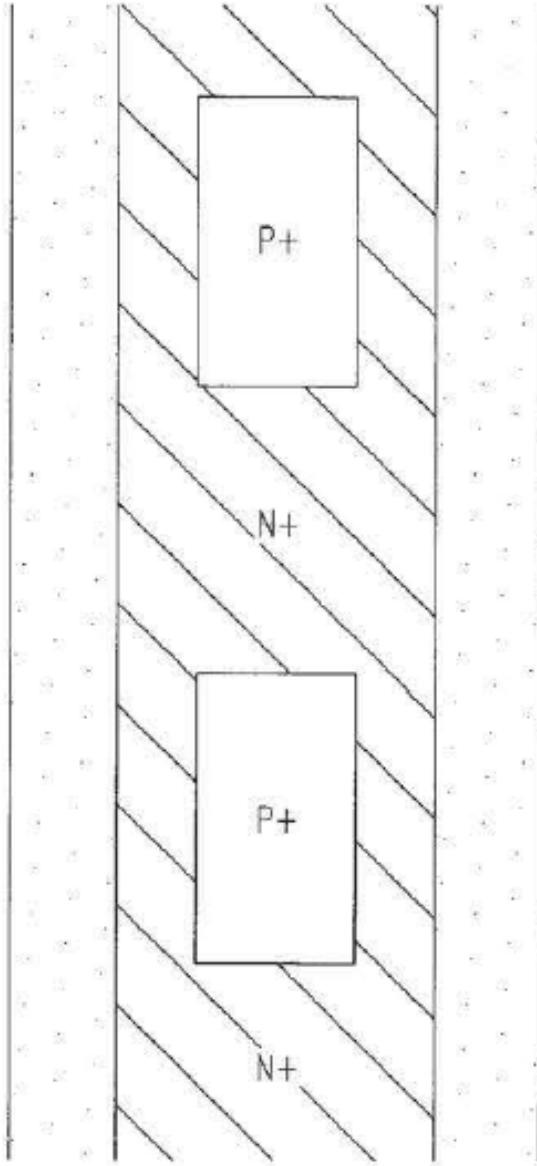


FIG. 19E

Ex. 1004, Fig. 19E. Figure 19E “shows a continuous N⁺ source region with P⁺ body contact ‘windows.’” *Id.* at 10:23–25, 16:63–65. Williams explains that “the window and strapped window based designs of FIGS. 19E and 19F

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have similar geometric features to the corrugated and strapped corrugated designs of FIGS. 19A and 19B, respectively, but with better N⁺ contact resistance and less P⁺ contact area (less rugged).” *Id.* at 17:15–19.

B. Level of Ordinary Skill in the Art

The level of ordinary skill in the art is a factual determination that provides a primary guarantee of objectivity in an obviousness analysis. *Al-Site Corp. v. VSI Int'l Inc.*, 174 F.3d 1308, 1324 (Fed. Cir. 1999) (citing *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966); *Ryko Mfg. Co. v. Nu-Star, Inc.*, 950 F.2d 714, 718 (Fed. Cir. 1991)). In determining the level of skill in the art, we consider evidence of the type of problems encountered in the art, the prior art solutions to those problems, the rapidity with which innovations are made, the sophistication of the technology, and the educational level of active workers in the field. *Custom Accessories, Inc. v. Jeffrey-Allan Indus. Inc.*, 807 F.2d 955, 962 (Fed. Cir. 1986); *Orthopedic Equip. Co. v. U.S.*, 702 F.2d 1005, 1011 (Fed. Cir. 1983).

Petitioner directs us to Dr. Subramanian’s opinion that a person of ordinary skill in the relevant technical field at the time of the invention “would have had the equivalent of a Bachelor’s [D]egree in electrical engineering or a related subject and two or more years of experience in the field of semiconductor devices.” Pet. 3; Ex. 1002 ¶ 23. In Petitioner’s and Dr. Subramanian’s further view, “Less work experience may be compensated by a higher level of education, such as a Master’s Degree, and vice versa.” Pet. 3; Ex. 1002 ¶ 23.

Patent Owner counters that “Petitioner’s asserted level of skill in the art is absurdly low given the silicon carbide technology” that is the subject of the ’633 patent. Prelim. Resp. 15. In Patent Owner’s view, the ordinarily

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skilled artisan would have possessed a Master’s Degree in electrical engineering or a related field “with a concentration in design and fabrication of silicon carbide power semiconductor devices” or a Bachelor’s Degree in electrical engineering or a related field combined with “two years of experience in design and fabrication of silicon carbide power semiconductor devices.” *Id.* at 16. Patent Owner directs us to evidence that “[t]his level of ordinary skill is consistent with the specialized nature of the field of silicon carbide power semiconductor devices.” *Id.*; Ex. 2004, x. Patent Owner further advances evidence that the ’633 patent inventors, as well as a “few others who were active in the highly specialized field of silicon carbide power devices,” possessed backgrounds consistent with Patent Owner’s proposed narrower definition of the level of ordinary skill. Prelim. Resp. 17–18; Ex. 2007, 1–2; Ex. 2017, 1; Ex. 2018, 1; Ex. 2019, 1–2.

On this record, we determine that the level of ordinary skill is reflected in the prior art of record. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (specific findings on the ordinary skill level are not required “where the prior art itself reflects an appropriate level and a need for testimony is not shown” (quoting *Litton Indus. Prods., Inc. v. Solid State Sys. Corp.*, 755 F.2d 158, 163 (Fed. Cir. 1985))). A more specific definition is not necessary, for purposes of deciding whether to institute review, at least because neither party explains how the result would change based on our selection of a definition. To the extent a more specific definition is required, however, we adopt Petitioner’s proposed definition because, on this record, it is consistent with the disclosures of the asserted prior art references. In any event, for the reasons explained below, even under Petitioner’s broader definition, Petitioner fails to establish a reasonable likelihood of prevailing

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at trial with respect to any challenged claim based on the ground of unpatentability advanced in the Petition.

C. Claim Construction

In an *inter partes* review, we construe a claim in an unexpired patent “in accordance with the ordinary and customary meaning of such claim as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.” 37 C.F.R. § 42.100(b) (2020). “[T]he ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention.” *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) (en banc). “Importantly, the person of ordinary skill in the art is deemed to read the claim term not only in the context of the particular claim in which the disputed term appears, but in the context of the entire patent, including the specification.” *Id.*

We agree with the parties that no claim term requires express construction for purposes of this Decision. Pet. 38–39; Prelim. Resp. 18–19; see *Wellman, Inc. v. Eastman Chem. Co.*, 642 F.3d 1355, 1361 (Fed. Cir. 2011) (“[C]laim terms need only be construed ‘to the extent necessary to resolve the controversy.’”). To the extent the scope of any claim term requires discussion, however, we provide it in the next subsection.

D. Reasons to Combine References

Petitioner asserts that claims 9–11 are unpatentable as obvious based on the combined disclosures of Ryu and Williams. Pet. 4. The challenge rests on Petitioner’s assertions that a person of ordinary skill in the art would have been prompted to modify Ryu’s MOSFET to include features disclosed in Williams. *Id.* at 39–82.

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Petitioner relies on Ryu for disclosures of a MOSFET having a silicon-carbide substrate, a drift semiconductor layer formed on a front side of that substrate, and a first source region as specified in claim 9. Pet. 39–46. Petitioner acknowledges that Ryu, however, does not disclose other features of claim 9, which are inherited by claims 10 and 11 through dependence from claim 9. *Id.* at 46–77. We expressly limit this Decision to the dispositive question whether Petitioner articulates adequate reasons why an ordinarily skilled artisan would have modified Ryu’s MOSFET to include a “first source electrode defining a longitudinal axis,” where “each of [a] plurality of first base contact regions” is “spaced apart from each other in a direction parallel to” that longitudinal axis. Ex. 1001, 9:47–53.

Petitioner acknowledges that those features are not disclosed in Ryu’s device, but asserts that an ordinarily skilled artisan “would have been motivated to use Williams’ teachings of multiple and periodic P⁺ body contact regions in Ryu to maximize the contact of the [P]⁺ regions and ruggedize Ryu’s MOSFET.” Pet. 69. In particular, Petitioner argues a person of ordinary skill in the art would have imported into Ryu’s MOSFET the “contact windows” disclosed in Williams’ Figure 19E (reproduced *supra* 13) to achieve a device within the scope of a challenged claim. Pet. 70. For the reasons discussed below, on the record presented, we determine that Petitioner’s rationale for this proposed combination is insufficient.

According to Petitioner, the design illustrated in Williams’ Figure 19E would have been understood to “help reduce on-resistance,” while simultaneously working “to ruggedize Ryu’s MOSFET against unwanted activation of parasitic” bipolar junction transistor (“BJT”) formation between the source, body, and drain. *Id.* Patent Owner responds, and we

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agree, that “instead of promoting ruggedness,” the design illustrated in Williams’ Figure 19E “sacrifice[s] ruggedness for better N⁺ contact resistance.” Prelim. Resp. 41–42 (citing Ex. 1004, 17:15–19 (Williams’ disclosure that the design illustrated in Figure 19E provides a “less rugged” device “with better N⁺ contact resistance and less P⁺ contact area”)).

In particular, Williams discloses that the Figure 19E design maximizes “the N⁺ source perimeter,” whereas a different design is employed to “suppress parasitic bipolar turn-on” and improve ruggedness. Ex. 1004, 16:29–35. Against that backdrop, we agree with Patent Owner that Williams improves ruggedness and suppresses parasitic BJT formation, not by the design shown in Figure 19E, but by a different design illustrated in Figure 19C. Notably, Petitioner does not explicitly rely on the embodiment in Figure 19C, as it is characterized by a “segmented N⁺ source design” and lacks the “plurality of” base contact regions of claim 9. Prelim. Resp. 43; *see* Ex. 1004, Fig. 19C (reproduced *supra* 12), 16:28–35, 17:15–19.

Nevertheless, Petitioner repeatedly asserts that an ordinarily skilled artisan would have combined the disclosures of Ryu and Williams in the manner claimed in pursuit of improved ruggedness and suppression of parasitic BJT formation. Pet. 11–16, 37–38, 52–56, 61–71. Those assertions are “expressly refuted by” disclosures in “Williams itself,” regarding the embodiment shown in Figure 19E, which Petitioner relies upon for its proposed combination. Pet. 70; Prelim. Resp. 41; Ex. 1004, Fig. 19E, 16:28–35, 17:19. In other words, Petitioner proposes reasons for the combination of Ryu and Williams that run counter to clear disclosures within the four corners of the asserted prior art. On this record, therefore, we detect in Petitioner’s rationale the taint of impermissible “hindsight”

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reconstruction. Prelim. Resp. 41; *compare* Pet. 70 (asserting that Williams' Figure 19E would have prompted the proposed modification "to ruggedize Ryu's MOSFET against unwanted activation of parasitic BJT"), *with* Ex. 1004, 16:28–36, 17:15–19 (Williams, indicating that Figure 19E produces a "less rugged" device that sacrifices "parasitic bipolar turn-on").

To the extent Petitioner proposes that Williams' Figure 19E discloses a known, interchangeable, alternative design element, which an ordinarily skilled artisan would have recognized as sharing a function in common with a design element of Ryu's device, that proposition is neither developed adequately in the Petition nor supported sufficiently by objective evidence of "predictable results." Pet. 71–72 (arguing, in conclusory fashion, that the proposed modification represents "a simple substitution of one known element . . . for another . . . to obtain predictable results") (citing Ex. 1002 ¶ 124 (Dr. Subramanian, repeating that conclusory factual proposition without directing the Board to any objective supporting evidence)). That conclusory proposition is of little probative value. *Id.*; *see Ashland Oil, Inc. v. Delta Resins & Refractories, Inc.*, 776 F.2d 281, 294 (Fed. Cir. 1985) (a "[l]ack of factual support for" opinion testimony, going to a factual determination, "may render the testimony of little probative value").

Petitioner further asserts that incorporation of the contact windows shown in Williams' Figure 19E into Ryu's MOSFET "would have been obvious to try" because Williams illustrates "at least six" design choices, in Figures 19A–19F, for forming adjacent N⁺ and P⁺ regions. Pet. 72. In that regard, Petitioner argues that an ordinarily skilled artisan "**could have pursued**" each choice disclosed in Williams, including the design depicted in Figure 19E, "because the analysis would have simply involved trying each

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one” in Ryu’s MOSFET as a matter of “simple design choice.” *Id.* (Board’s emphasis). On that point, however, we agree with Patent Owner that Petitioner, at best, shows only that an ordinarily skilled artisan “***could have*** made the” proposed substitution, without explaining adequately why one ***would have*** done so, in view of Williams’ clear teachings that the design illustrated in Figure 19E ***sacrifices*** ruggedness, making the device “less rugged,” and ***sacrifices*** the “parasitic bipolar turn-on” suppression in favor of achieving “the lowest possible resistance.” Ex. 1004, 16:28–35, 17:15–19; *see* Prelim. Resp. 42–43 (and citations therein to evidence and authority).

In a nutshell, Petitioner’s extensive reliance on improved ruggedness of the MOSFET and suppression of parasitic BJT formation, as reasons supporting the proposed modification of Ryu’s device in view of Williams’ Figure 19E, is undercut by clear disclosures in Williams. Pet. 11–16, 37–38, 52–56, 61–71 (extensive reliance); Ex. 1004, 16:28–35, 17:15–19 (Williams’ clear disclosures). On this record, therefore, Petitioner’s rationale for the combination appears to be driven, not by the disclosures of the prior art but, instead, by an exercise of impermissible hindsight reconstruction. *Compare* Pet. 71–73, *with* Prelim. Resp. 41–43. Thus, we agree with Patent Owner that Petitioner’s “rationale for combining the teachings of Ryu and Williams” in the manner claimed is “flawed.” Prelim. Resp. 43.

That deficiency undermines the ground of unpatentability set forth in the Petition. *See* Pet. 4 (identification of challenge). Petitioner does not show a reasonable likelihood of prevailing with respect to any challenged claim.

IV. CONCLUSION

Based on the information presented in the Petition and the Preliminary Response, we deny the Petition and do not institute an *inter partes* review.

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V. ORDER

It is

ORDERED that the Petition is *denied* and no *inter partes* review is instituted.

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For PETITIONER:

Richard Goldenberg
Scott Bertulli
Trishan Esram
WILMER CUTLER PICKERING HALE AND DORR LLP
Richard.goldenberg@wilmerhale.com
Scott.bertulli@wilmerhale.com
Trishan.esram@wilmerhale.com

For PATENT OWNER:

Michelle Armond
Douglas Wilson
Josepher Li
ARMOND WILSON LLP
Michelle.armond@armondwilson.com
doug.wilson@armondwilson.com
josepher.li@armondwilson.com